Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus for selecting test patterns comprising:

a first test pattern selecting module configured to classify a plurality of verification patterns of a logic circuit of an LSI into a plurality of selected test patterns fulfilling a reliability criterion and a plurality of unselected test patterns failing to fulfill the reliability criterion;

a fault simulation module configured to simulate whether the plurality of selected test patterns and the plurality of unselected test patterns detect a plurality of faults estimated to occur in the logic circuit;

a weighting module configured to add weight reflecting a plurality of layout elements of the logic circuit **and information on each name of the plurality of layout elements** to each of a plurality of first undetected faults that are undetected by the plurality of selected test patterns and define the plurality of first undetected faults **to which** ~~that are given~~ the ~~weight~~ **weights are given** as a plurality of first weighted undetected faults;

a fault sampling module configured to extract a plurality of second undetected faults from the plurality of first weighted undetected faults; ~~and~~

a second test pattern selecting module configured to extract a plurality of additionally selected test patterns that detects ~~complementarily~~ the plurality of second undetected faults ~~from each other~~ from the plurality of **the** unselected test patterns based on a criterion of the added weight~~.~~**; and**

a data memory configured to store a plurality of final weighted undetected faults among from the plurality of first weighted undetected faults, the plurality of final weighted undetected faults being not detected by the plurality of additionally selected test patterns.

2. (Currently Amended) **An apparatus for selecting test patterns comprising:**

a first test pattern selecting module configured to classify a plurality of verification patterns of a logic circuit of an LSI into a plurality of selected test patterns fulfilling a

reliability criterion and a plurality of unselected test patterns failing to fulfill the reliability criterion;

a fault simulation module configured to simulate whether the plurality of selected test patterns and the plurality of unselected test patterns detect a plurality of faults estimated to occur in the logic circuit;

a weighting module configured to add weight reflecting a plurality of layout elements of the logic circuit to each of a plurality of first undetected faults that are undetected by the plurality of selected test patterns and define the plurality of first undetected faults to which the weights are given as a plurality of first weighted undetected faults;

a fault sampling module configured to extract a plurality of second undetected faults from the plurality of first weighted undetected faults; and

a second test pattern selecting module configured to extract a plurality of additionally selected test patterns that detects the plurality of second undetected faults from the plurality of the unselected test patterns based on a criterion of the added weight.

~~The apparatus of claim 1,~~ wherein the second test pattern selecting module further ~~comprising~~ **comprises**:

a candidate test pattern selecting module configured to select a plurality of candidate test patterns that detect the plurality of second undetected faults from the plurality of unselected test patterns based on a first criterion of an evaluation value reflecting the added weight among the plurality of second undetected faults of detected faults by each of the plurality of unselected test patterns and a pattern length of each of the plurality of the unselected test patterns; and

an additionally selected test pattern selecting module configured to exclude from processing the plurality of candidate test patterns failing to fulfill a second criterion of the evaluation value and select an additionally selected test pattern by which the evaluation value is a maximum from the plurality of candidate test patterns and exclude from processing among the plurality of second undetected faults detected faults by the additionally selected test pattern and update the evaluation value**, the additionally selected test pattern being one of the plurality of additionally selected test patterns**.

3. (Currently Amended) A computer implemented method for selecting test patterns comprising:

classifying a plurality of verification patterns of a logic circuit of an LSI into a plurality of selected test patterns fulfilling a reliability criterion and a plurality of unselected test patterns failing to fulfill the reliability criterion;

simulating whether the plurality of selected test patterns detects a plurality of faults estimated to occur in the logic circuit;

adding a weight reflecting a plurality of layout elements of the logic circuit **and information on each name of the plurality of layout elements** to each of a plurality of first undetected faults that are undetected by the plurality of selected test patterns and defining the plurality of first undetected faults **to which the weights are added** ~~that are added the weights~~ as a plurality of first weighted undetected faults;

extracting a plurality of second undetected faults from the plurality of first weighted undetected faults based on an extracting condition;

simulating whether the plurality of unselected test patterns detects the plurality of second undetected faults; ~~and~~

selecting a plurality of additionally selected test patterns that detects ~~complementarily~~ the plurality of second undetected faults ~~from each other~~ from the plurality of **the** unselected test patterns based on a criterion of the added weight.; **and**

listing a plurality of final weighted undetected faults among from the plurality of first weighted undetected faults, the plurality of final weighted undetected faults being not detected by the plurality of additionally selected test patterns.

4. (Original) The computer implemented method of claim 3, wherein the reliability criterion is a functional verification coverage.

5. (Original) The computer implemented method of claim 3, wherein the reliability criterion is a coverage of the plurality of faults.

6. (Original) The computer implemented method of claim 3, wherein the extracting condition is a random sampling.

7. (Currently Amended) The computer implemented method of claim 3, wherein the extracting condition is a value proportional to the added weight.

8. (Currently Amended) **A computer implemented method for selecting test patterns comprising:**

classifying a plurality of verification patterns of a logic circuit of an LSI into a plurality of selected test patterns fulfilling a reliability criterion and a plurality of unselected test patterns failing to fulfill the reliability criterion;

simulating whether the plurality of selected test patterns detects a plurality of faults estimated to occur in the logic circuit;

adding a weight reflecting a plurality of layout elements of the logic circuit to each of a plurality of first undetected faults that are undetected by the plurality of selected test patterns and defining the plurality of first undetected faults to which the weights are added as a plurality of first weighted undetected faults;

extracting a plurality of second undetected faults from the plurality of first weighted undetected faults based on an extracting condition;

simulating whether the plurality of unselected test patterns detects the plurality of second undetected faults; and

selecting a plurality of additionally selected test patterns that detects the plurality of second undetected faults from the plurality of the unselected test patterns based on a criterion of the added weight,

~~**The computer implemented method of claim 3,**~~ wherein ~~**the**~~ selecting ~~**a**~~ **the** plurality of additionally selected test patterns further ~~**comprising**~~ **comprises**:

selecting a plurality of candidate test patterns that detect the plurality of second undetected faults from the plurality of unselected test patterns based on a first criterion of an evaluation value reflecting the added weight among the plurality of second undetected faults of detected faults by each of the plurality of unselected test patterns and a pattern length of each of the plurality of the unselected test patterns;

excluding from processing the plurality of candidate test patterns failing to fulfill a second criterion of the evaluation value;

extracting an additionally selected test pattern by which the evaluation value is a maximum from the plurality of candidate test patterns, **the additionally selected test pattern being one of the plurality of additionally selected test patterns**; and

excluding from processing among the plurality of second undetected faults detected faults by the additional selected test pattern and updating the evaluation value.

9. (Currently Amended) A computer program product for controlling a computer system so as to select test patterns, the computer program product comprising:

a recording medium readable by the computer system;

instructions **recorded on the recording medium for directing the computer system** ~~configured~~ to classify a plurality of verification patterns of a logic circuit of an LSI into a plurality of selected test patterns fulfilling a reliability criterion and a plurality of unselected test patterns failing to fulfill the reliability criterion ~~within the computer system~~;

instructions **recorded on the recording medium for directing the computer system** ~~configured~~ to simulate whether the plurality of selected test patterns detects a plurality of faults estimated to occur in the logic circuit ~~within the computer system~~;

instructions **recorded on the recording medium for directing the computer system** ~~configured~~ to add a weight reflecting a plurality of layout elements of the logic circuit **and information on each name of the plurality of layout elements** to each of a plurality of first undetected faults that are undetected by the plurality of selected test patterns and define the plurality of first undetected faults **to which the weights are added** ~~that are added the weights~~ as a plurality of first weighted undetected faults ~~within the computer system~~;

instructions **recorded on the recording medium for directing the computer system** ~~configured~~ to extract a plurality of second undetected faults from the plurality of first weighted undetected faults based on an extracting condition ~~within the computer system~~;

instructions **recorded on the recording medium for directing the computer system** ~~configured~~ to simulate whether the plurality of unselected test patterns detects the plurality of second undetected faults ~~within the computer system; and~~

instructions **recorded on the recording medium for directing the computer system** ~~**configured**~~ to select a plurality of additionally selected test patterns that detects ~~**complementarily**~~ the plurality of second undetected faults ~~**from each other**~~ from the plurality of **the** unselected test patterns based on a criterion of the added weight ~~**within the computer system.**~~**; and**

instructions recorded on the recording medium for directing the computer system to list a plurality of final weighted undetected faults among from the plurality of first weighted undetected faults, the plurality of final weighted undetected faults being not detected by the plurality of additionally selected test patterns.

10. (Original) The computer program product of claim 9, wherein the reliability criterion is a functional verification coverage.

11. (Original) The computer program product of claim 9, wherein the reliability criterion is a coverage of the plurality of faults.

12. (Original) The computer program product of claim 9, wherein the extracting condition is a random sampling.

13. (Original) The computer program product of claim 9, wherein the extracting condition is value proportional to the added weight.

14. (Currently Amended) **A computer program product for controlling a computer system so as to select test patterns, the computer program product comprising:**

a recording medium readable by the computer system;

instructions recorded on the recording medium for directing the computer system to classify a plurality of verification patterns of a logic circuit of an LSI into a plurality of selected test patterns fulfilling a reliability criterion and a plurality of unselected test patterns failing to fulfill the reliability criterion;

instructions recorded on the recording medium for directing the computer system to simulate whether the plurality of selected test patterns detects a plurality of faults estimated to occur in the logic circuit;

instructions recorded on the recording medium for directing the computer system to add a weight reflecting a plurality of layout elements of the logic circuit to each of a plurality of first undetected faults that are undetected by the plurality of selected test patterns and define the plurality of first undetected faults to which the weights are added as a plurality of first weighted undetected faults;

instructions recorded on the recording medium for directing the computer system to extract a plurality of second undetected faults from the plurality of first weighted undetected faults based on an extracting condition;

instructions recorded on the recording medium for directing the computer system to simulate whether the plurality of unselected test patterns detects the plurality of second undetected faults; and

instructions recorded on the recording medium for directing the computer system to select a plurality of additionally selected test patterns that detects the plurality of second undetected faults from the plurality of the unselected test patterns based on a criterion of the added weight.

~~**The computer program product of claim 9,**~~ wherein the second extracting instructions further ~~**comprising**~~ **comprises**:

instructions **recorded on the recording medium for directing the computer system** ~~**configured**~~ to extract a plurality of candidate test patterns that detect the plurality of second undetected faults from the plurality of unselected test patterns based on a first criterion of an evaluation value reflecting the added weight among the plurality of second undetected faults of detected faults by each of the plurality of unselected test patterns and a pattern length of each of the plurality of the unselected test patterns ~~**within the computer system**~~;

instructions **recorded on the recording medium for directing the computer system** ~~**configured**~~ to exclude from processing the plurality of candidate test patterns failing to fulfill a second criterion of the evaluation value ~~**within the computer system**~~;

instructions **recorded on the recording medium for directing the computer system** ~~**configured**~~ to select an additionally selected test pattern by which the evaluation value is a maximum from the plurality of candidate test patterns ~~**within the computer system**~~**, the additionally selected test pattern being one of the plurality of additionally selected test patterns**; and

instructions **recorded on the recording medium for directing the computer system** ~~**configured**~~ to exclude from processing among the plurality of second undetected faults detected faults by the additional selected test pattern and update the evaluation value ~~**within the computer system**~~.